In the Claims:

Claims 1-12 (canceled)

Claim 13-20

13. (Original) A method of making a symmetric transistor device comprising: depositing a first conductive layer on a substrate, the first conductive layer forming an even number of transistor legs, laid out in an intersecting pattern, forming a bilaterally symmetric base;
doping the substrate to form source and drain regions; and
forming a plurality of transistors defined by a portion of a leg forming a gate and the source and drain areas on either side of the leg forming a source and a drain.

14. (Original) The method of claim 13, further comprising: depositing a silicon dioxide prior to depositing the first conductive layer.

15. (Original) The method of claim 13, wherein a diffusion plate used for doping forms undoped areas at intersections of the transistor legs.

16. (Original) The method of claim 13, wherein the intersecting pattern forms a tic-tac-toe pattern.

17. (Original) The method of claim 13, wherein the first conductive layer comprises polysilicon.

18 (Original) The method of claim 13, further comprising:

conductive interconnections between the source and drain areas to form a circuit.

19. (Original) The method of claim 13, wherein a first half of the transistors are oriented along a first axis and a second half of the transistors (N/2) oriented along a second axis orthogonal to the first half of the transistors.

20. (Original) The method of claim 19, wherein the minimum drawn W/L is used for each transistor leg.